

# CML Current mode full adders for 2.5-V power supply

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## Abstract

We present the basic structure and performance of CML current mode full adders, that are used as Carry Save Adders (CSA) in combinatorial multipliers. A 1.2  $\mu\text{m}$  BiCMOS technology is used for simulations but the schematic assumes a 2.5-V power supply. Compared with binary voltage mode CSAs, the multivalued current mode CSAs have chip area and power dissipation advantage, but speed disadvantage. The current mode version is far more sensitive to power supply and temperature shifts.

It is widely acknowledged that the binary circuits have better performance than the multivalued ones [1]. However, there exist some cases where multivalued circuits could be interesting. For many years, multivalued current-mode circuits have been considered as potential candidates to implement efficiently arithmetic functions. As an example, a 2  $\mu\text{m}$  current-mode CMOS 32 x 32 bit multiplier [2] has been demonstrated, with the same speed and half chip area and power dissipation compared with the best corresponding binary one at the same period. A potential drawback of current mode circuit is that fan-out is one. This is not a problem in the multioperand addition which is the critical path to implement combinatorial multipliers.

In this paper, we present a current mode CML 1 bit full adder which can be used as a Carry Save Adder in the reduction tree of a multiplier. It only uses bipolar transistors and resistors, but it is suitable to be used with a BiCMOS technology, where CML circuits are mixed with CMOS circuits. Although we use the simulation parameters and the layout design rules of a 1.2  $\mu\text{m}$  BiCMOS technology of SGS-Thomson, we only consider circuitry that will be usable with advanced BiCMOS technologies, using reduced power supply voltages. Our CML current mode adder is designed with a 2.5-V power supply. The main features of the technology are given in table 1.

Speed, power dissipation and device complexity are compared for the current mode multivalued full adder and the binary voltage mode full adder that can be designed with the same power supply.

## 2. Four-valued CML circuitry for 1-bit adder

### 2.1. Basic building blocks

CMOS	NPN
NMOS (50/50) $V_{th} : 0.7\text{V}$	Se : 3.6 x 3.6 $\mu\text{m}^2$
PMOS (50/50) $V_{th} : 1.0\text{V}$	hfe : 90
BVDSS > 7V	BVCEO : 14V
td (fin=fout) : 220 ps	BVCBO : 25 V
	BVEBO : 5V
	VEA : 50 V
	Ceb : 37.5 fF
	Ccb : 27 fF
	Ccs : 106 fF
	rbb' : 370 $\Omega$
	ft max : 8 GHz

Table 1 : HF3CMOS Technology

The basic cell is called 4-BC (4 valued input current to binary outputs converter). It is used to implement the current mode 1-bit adder, according to figure 1. Three binary current inputs are summed and the analog sum is decomposed according to sum and carry binary current outputs (Table 2)

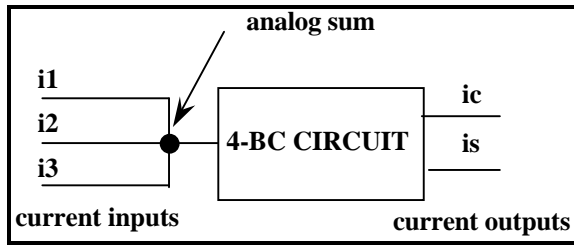


Figure 1 : current mode 1-bit adder

$\Sigma i$	$i_c$	$i_s$
0	0	0
1	0	1
2	1	0
3	1	1

Table 2

The 4-BC cell uses three different threshold detectors, implementing the  $G_j$  (greater) and  $L_j$  (less) binary functions that are defined below and presented in table 3.

$G_j(i) = 1$  if  $i > j$ ;  $G_j(i) = 0$  otherwise

$L_j(i) = 1$  if  $i \leq j$ ,  $L_j(i) = 0$  otherwise.

According to the definition,  $L_j = \overline{G_j}$

The outputs are easily expressed as a function of the  $G_j$  and  $L_j$  functions (table 3).

$i_y = G_1(i)$

$i_x = G_0(i).L_1(i) + G_2(i)$

$i$	$G_0$	$G_1$	$G_2$	$L_0$	$L_1$	$L_2$	$i_c$	$i_s$
0	0	0	0	1	1	1	0	0
1	1	0	0	0	1	1	0	1
2	1	1	0	0	0	1	1	0
3	1	1	1	0	0	0	1	1

Table 3:  $G_j$  and  $L_j$  functions

## 2.2. Design with a 2.5 V power supply.

The power supply voltage is 2.5V. The current unit is  $I = 400 \mu A$ , which corresponds approximately to the best speed x power trade-off for the HCMOS3 technology when it is used to implement CML-ECL differential pairs. The voltage drop  $\Delta V = RI$  associated to each current unit is chosen as 0.3V. We assume that the base emitter voltage drop is  $V_{be} = 800 mV$

The  $G_j$  and  $L_j$  threshold detectors are shown in figure 2. Table 4 gives the voltage levels in A and B for each input value.

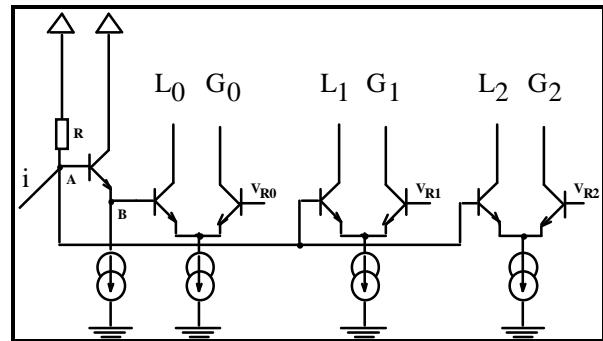


Figure 2: Threshold detectors

	A	B
0	2.5V	1.7V
1	2.2V	1.4V
2	1.9V	1.1V
3	1.6V	0.8V

Table 4: Voltage levels

The voltage reference values are deduced from table 4.

$V_{R0} = 1.55 V$

$V_{R1} = 2.05 V$

$V_{R2} = 1.75 V$

It should be noticed that  $G_0$  comparison is done with B level, after a  $V_{be}$  shift, to avoid saturation of the right transistor of the pair when using  $G_0$  output. This output is connected to a summing resistor, with a maximum  $3I$  current which gives 0.9V voltage drop and a 1.6V output.

The overall schematic of the 4-BC cell is presented in figure 3.  $G_0(i).L_1(i)$  function is implemented by the two parallel transistors on the left side of the differential pair biased by voltage value  $V_{R0}$ . The reference circuits are presented in figure 4.

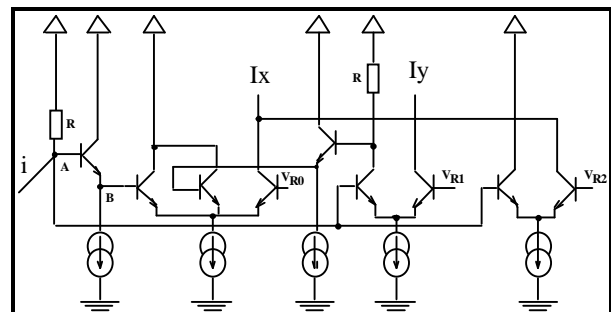
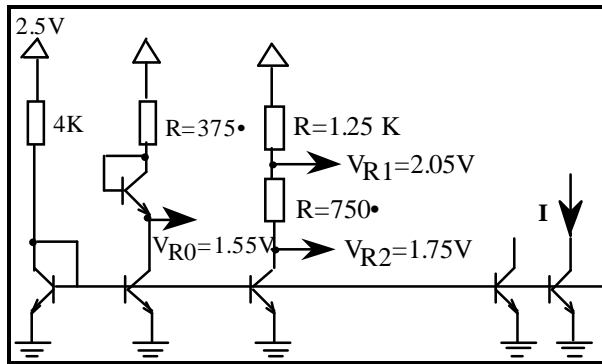


Figure 3: 4-BC cell schematic.



**Figure 4: Reference circuits.**

The reference circuits use current mirrors to deliver about 20 differential pairs and the voltage reference. The current source  $I$  is very sensitive to any supply voltage shift. It is fundamental that  $V_{R2}$  threshold value, that is compared with  $B$  voltage which is either  $V_{CC} - 2RI$  or  $V_{CC} - 3RI$ , to be  $V_{CC} - 2.5 RI$ . It is the same for  $V_{R1}$  value. On the other hand,  $V_{R0}$  threshold value is compared to  $V_{CC} - V_{be} - 0.5 RI$  or  $V_{CC} - V_{be} - RI$ . It should be  $V_{CC} - V_{be} - 0.25 RI$ .

### 2.3. Performance

The sum and carry propagation delays are given in Table 5 and 6. They correspond to circuits with fan-out =1 and a 0.2 pF interconnection capacitance. The worst cases are considered, both in power supply voltage shift (+/- 10%) and in temperature (0°C to 70°C). The adder is used as a Carry Save Adder (CSA), for which both sum and carry delays are important. From Table 5 and 6, we can deduce that the CSA delay is 2.2 ns for nominal case, and 4.2 ns for the worst case (2.25-V and 0°C).

Temp	$V_{CC}=2.25$ V	$V_{CC}=2.5$ V	$V_{CC}=2.75$ V
0°	4.2 ns	2.4 ns	2.2 ns
27°	3.6 ns	2.2 ns	2.0 ns
70°	3.2 ns	1.8 ns	1.6 ns

**Table 5: current mode full adder sum delay**

Temp	$V_{CC}=2.25$ V	$V_{CC}=2.5$ V	$V_{CC}=2.75$ V
0°	2.2ns	1.8ns	1.6 ns
27°	2.0 ns	1.6 ns	1.4 ns
70°	1.6 ns	1.4 ns	0.8ns

**Table 6: current mode full adder carry delay**

The current mode full adder uses 2 differential pairs, two emitter followers and the current reference circuit.

The overall current per full adder is 2 mA, which gives a nominal power dissipation of 5 mW. The voltage reference circuit uses 1.2  $\mu$ A and dissipates 3 mW. If we assume that this circuit delivers 20 adders, the average nominal power dissipation is 5.15 mW.

The nominal speed x power dissipation factor is close to 11.5 pJ. For worst case, it is close to 19.5 pJ.

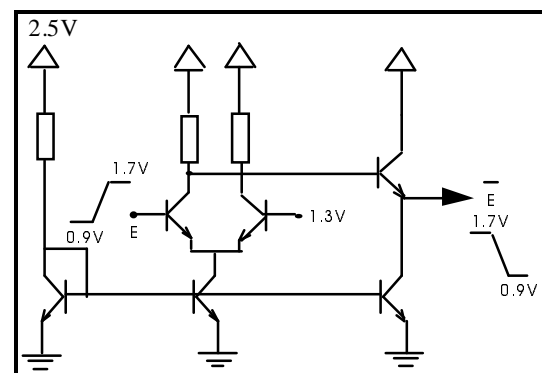
The full adder uses 14 transistors and 2 resistors. The reference circuit uses 4 transistors and 4 resistors. The average number of devices per CSA is thus 14.2 T and 2.2 R.

## 3. Binary voltage mode ECL circuitry for 1-bit adder

For comparison, we now consider a binary voltage mode version of the full adder, that uses the same 2.5 V power supply. With CML-ECL circuits, series-gating cannot be used with 2.5V power supply. To keep logic flexibility, we use the same approach as in [3]. With 0.8 V logic swing, wire-anding can be used with a standard technology without Schottky diodes. Wire-oring can be used if emitter followers are available (ECL levels are used instead of CML levels).

### 3.1. Voltage mode design

Figure 5 presents the inverter circuit. Voltage levels are 1.7 V and 0.9 V. The usual ECL techniques can be used to implement the Nor or Or functions. The current source of the ECL circuit is implemented by a bipolar current mirror, which allows the circuit to operate with a 2.5 V supply. The reference voltage is carefully chosen to be 1.3 V to avoid saturation of the current source transistor. The corresponding circuit is presented in Figure 6. The current sources deliver 400  $\mu$ A both for differential pairs and emitter followers.



**Figure 5: Basic inverter**

Figure 7 presents the circuit with collector dotting, which implements the and function. With  $a$  and  $b$  inputs, both  $a.b$  and  $\bar{a}.\bar{b}$  are obtained. The diodes are implemented with diode connected transistors. Figure 8 presents the emitter dotting, which implement the Or

function. When using both collector and emitter dottings in the circuit presented in Figure 7, we obtain the exclusive or function.

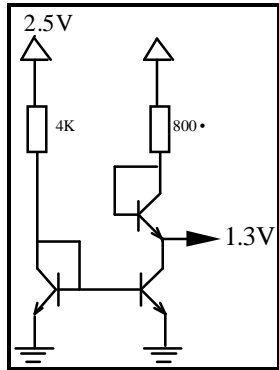


Figure 6: Reference circuit

The overall circuit for the full adder is presented in figure 9. It is important to notice that the propagation delays for carry and sum outputs is only two gate delays, as the emitter dottings do not introduce a significant delay.

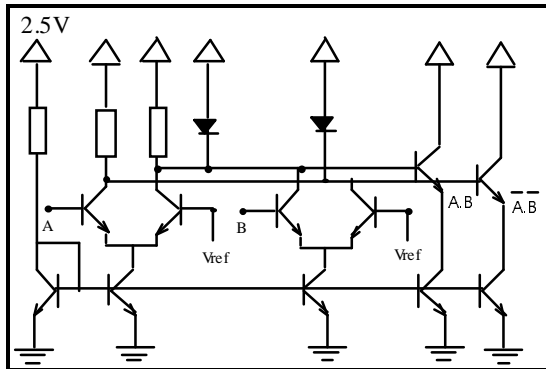


Figure 7: Collector dotting of ECL circuits

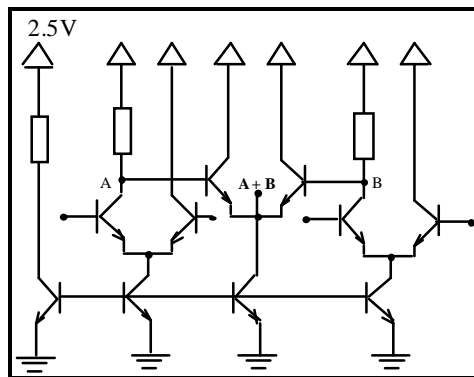


Figure 8: Emitter-dotting of ECL circuits

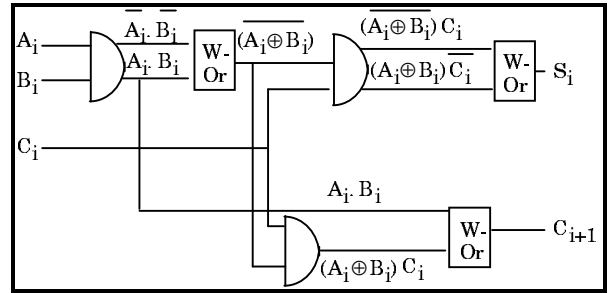


Figure 9: voltage mode 1-bit full adder

### 3.2. Performance

As for the current mode adder, we present the carry (Table 7) and sum (Table 8) propagation delays, for different voltage supply values and different temperature. We also assume a 0.2 pF capacitance on the carry and sum outputs, corresponding to wiring capacitances.

Temp	V <sub>CC</sub> =2.25 V	V <sub>CC</sub> =2.5 V	V <sub>CC</sub> =2.75 V
0°	825ps	750ps	700ps
27°	750ps	750ps	725ps
70°	800ps	700ps	675ps

Table 7: Carry input to output delay with 0.2 pF output capacitance

Temp	V <sub>CC</sub> =2.25 V	V <sub>CC</sub> =2.5 V	V <sub>CC</sub> =2.75 V
0°	1.2ns	1.2ns	1.2ns
27°	1.2ns	1.25ns	1.2ns
70°	1.3ns	1.25ns	1.1ns

Table 8: Sum input to output delay with 0.2 pF output capacitance

For the CSA, the nominal delay is 1.25 ns, and the worst case delay is 1.3 ns. The CSA delay is nearly insensitive to voltage and temperature shifts. The full adder uses 3 wired-and gates and 3 wired-or connections. Each wired-and gate uses 2 pairs. A wired-or connection uses a current unit. A current reference circuit is able to deliver the 9 current sources that are needed in the circuit. The CSA current is thus 4 mA and the power dissipation is 10 mW. The reference circuit uses 0.8 mA and dissipates 2 mW. If it delivers reference voltage for 20 adders, the average power dissipation per CSA is 10.1 mW.

The nominal speed x power dissipation factor is close to 12.7 pJ. For worst case, it is close to 13.1 pJ (this case corresponds to 2.75 V supply at 0°C).

The number of devices per function is 8T and 2R (wired-and), 3T (wired-or), 1T and 1R (current reference source) and 3T and 2R (voltage reference source). The number of devices is 34 T, 7 R for the full adder, and 3T, 2R for the voltage reference source. The average number of components per CSA is thus 34.15 T and 7.1 R.

#### 4. Overall comparison and concluding remarks

Table 9 gives the overall comparison between the 4-valued current mode CML adder and the corresponding binary voltage mode full adder using the same 2.5 V supply. Speed, power dissipation, speed x power dissipation, and the number of devices are compared. The actual layout has not been done.

	Typical	
	Current mode	Voltage mode
Delay	2.2 ns.	1.25 ns
Power dissipation	5.15 mW	10.1 mW
Speed x power dissipation	11.7 pJ	12.7 pJ
Transistors	14.2 T	34.15 T
Resistors	2.2 R	7.1 R

	Worst case	
	Current mode	Voltage mode
Delay	4.2 ns	1.3 ns
Power dissipation	5.66 mW	11,1 mW
Speed x power dissipation	19.5 pJ	13.1 pJ

The chip density advantage of the multivalued approach is significant, as it roughly uses 2.5 times less transistors and 3.5 times less resistors. The binary version is nearly two times faster for the nominal case, and three times faster for the worst case. The multivalued version power dissipation is two times less. As a result, the speed x power dissipation is slightly in favor of the multivalued version for the nominal case, but clearly in favor of the binary version for the worst case.

#### Figure 9: Overall comparison

Compared with the CMOS case [4], the comparison is more favorable to the CML-ECL multivalued circuits. The situation seems very typical of the multivalued circuits. They can exhibit some chip area or power dissipation advantages, but the speed comparison is always in favor of the binary voltage mode version. The multivalued current mode version is far more sensitive to power supply and temperature shifts. The voltage mode version is far more robust with parasitic effects (capacitive load, voltage supply and temperature shifts).

If CML-ECL multivalued circuits are “not too bad” with 2.5 V power supply, they are strictly limited to the 4-valued case, where they are working with very small voltage swing (300 mV). More, the speed advantage of CML circuits within a CMOS environment is more and more debatable versus a full CMOS version with the continuous progresses of CMOS technologies. It seems that there will not be promising future for CML-ECL multivalued circuits.

#### References

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