Performance of CMOS Current Mode Full Adders.

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Abstract

We present the performance of three different multivalued current mode 1-bit adders. These circuits have been simulated with the electrical parameters of a standard 1.2 µm CMOS technology. The performance of a binary voltage mode 1-bit adder is also presented. The binary version uses twice more transistors comparing with multivalued ones, but it is two or three times faster. Multivalued versions are more complicated to design and optimize. These results confirm the chip density advantage of multivalued circuits and the speed advantage of binary versions when using CMOS technologies.

1. Introduction

For many years, CMOS multivalued current mode circuits have been proposed [1-4], but most of them [1-3] used a standard CMOS technology. In 1986, a 2-µm current-mode CMOS 32 x 32 bit multiplier [5] has been demonstrated, with the same speed and half chip area and power dissipation compared with the best corresponding binary one at the same period. However, this chip used a non standard technology, with depleted pMOS transistors to implement current sources.

Multivalued current-mode circuits could be useful only if they can be implemented with **today** and **tomorrow** technologies. It means that they should be compatible with advanced CMOS, BiCMOS or CML-ECL bipolar technologies using reduced power supplies (3.3 V or 2V). It is highly desirable to use a standard advanced technology to keep the same IC process complexity.

The tolerance issue has always been the Achilles' heel of current-mode circuits [6]. To operate with m different current levels, m-1 threshold detectors are needed and the tolerance constraints are more and more difficult to satisfy when the number of current levels increases. We roughly know that 8 levels is an upper limit for many technologies. Multivalued circuits are the most efficient (speed, complexity) with 3 or 4 current levels.

In [7,8], we have set up the basis for a comparison of current mode multivalued circuits with voltage mode binary circuits for the multioperand addition that is required to perform high speed multiplication. 3-valued and 4-valued circuits have been defined for implementing 2-input and 3-input adders with the Borrow Save Carry redundant number representation, which is the number representation used in [9]. They are based on 3-valued to binary converter (3-BC) and 4-valued to binary converter (4-BC) circuits. These circuits are fundamental ones. Moreover, as we will detail, the 3-BC cell is the only cell that is needed to implement the current mode binary half-adder and the 4-BC cell is the only cell to implement the current-mode binary full adder.

In this paper, we will present the performance of various implementations of 4-BC circuits. It gives significant figures both for the comparison of voltage mode and current-mode versions of Carry-Save Adder of the binary world, and for the potentialities of using m-valued current mode cells ($m \leq 4$) in arithmetic operators based on redundant number systems.

2. Multivalued current-mode circuits

2.1. Basic building blocks

We use the following notations and definitions:
Let E_n be the digit set {0, 1, ..., n-1}.

$X, i \in E_m$, $L_i(X), G_i(x) \in E_2$

Current mode multivalued circuits have m different current levels, ranging from 0 to *m*-1. One basic operation is the analog sum of currents, which is free to implement. For m-valued circuits, the basic operators are the current sources, which deliver one given level of current, and the threshold detectors, which indicate if a current is greater or not than a given threshold value. The threshold detectors implement the binary functions L (Less or Equal) which have the following definition : $L_i(x) = 1$ iff $x \leq i$, and 0 otherwise. The binary functions G (Greater) are the binary complement of the

corresponding L functions : G_i (x) = 1 iff x > i, and 0 otherwise. Current mirrors are also needed to convert source to sink currents or sink to source currents.

The first implementation of current sources (figure 1) and threshold detectors (figure 2) with a standard CMOS technology has been presented by Freitas and Current in 1983 [2]. The current source value is determined by the diode-connected T_1 pMOS and T_2 nMOS transistors. T_4 is controlled by the voltage input c. When it is on, I is mirrored by T_1 and T_3. The threshold detectors compare a copy of the input current I_{in} (through T_5-T_7, T_5-T_9, T_5-T_{11}(current mirrors) with reference currents that are obtained by using T_1-T_6, T_1-T_8 and T_1-$T1_0$ current mirrors.

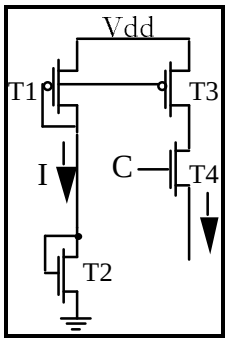


Figure 1 : CMOS current source.

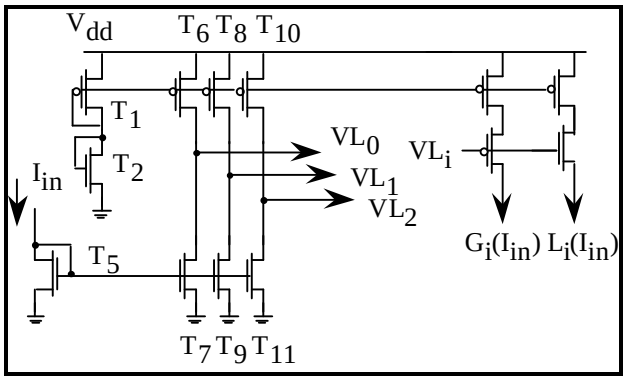


Figure 2 : CMOS threshold detectors

2.2. The m-BC cells

For m ≤ 4, the m-valued to binary converters deliver the binary outputs c_{i+1} and w_i corresponding to the m-valued input p_i according to the following definition :

$p_i = 2\ c_{i+1} + w_i$, where c_{i+1} and w_i, are respectively the carry and sum outputs.

The corresponding circuits are called m-BC. Tables1 and 2 give the truth table of the 3-BC and the 4-BC cells.

2.3. Digital implementation of m-BC cells

Digital implementation of m-BC cells is obtained when using threshold detector circuits and current sources, according to the following formulas for the 3-BC cell :

$c_{i+1} = G_1(p_i)$

$w_i = G_0(p_i).L_1(p_i)$

and for the 4-BC cell :

$c_{i+1} = G_1(p_i)$

$w_i = G_0(p_i).L_1(pi) + G_2(p_i)$.

In the last formula, the $G_0(p_i).L_1(pi)$ and $G_2(p_i)$ terms cannot be simultaneously equal to 1. + can be implemented as a logical Or or as an analog sum.

Functional schemes for these two circuits are given in Figure 3 and 4. These circuits are level-restoring.

p_i	c_{i+1}	w_i	$G_0(p_i)$	$G_1(p_i)$
0	0	0	0	0
1	0	1	1	0
2	1	0	1	1

Table 1 : 3-BC cell

p_i	c_{i+1}	w_i	$G_0(p_i)$	$G_1(p_i)$	$G_2(p_i)$
0	0	0	0	0	0
1	0	1	1	0	0
2	1	0	1	1	0
3	1	1	1	1	1

Table 2 : 4-BC cell

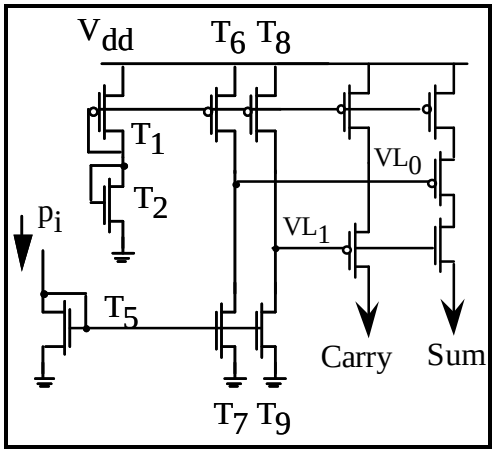


Figure 3 : 3-BC cell

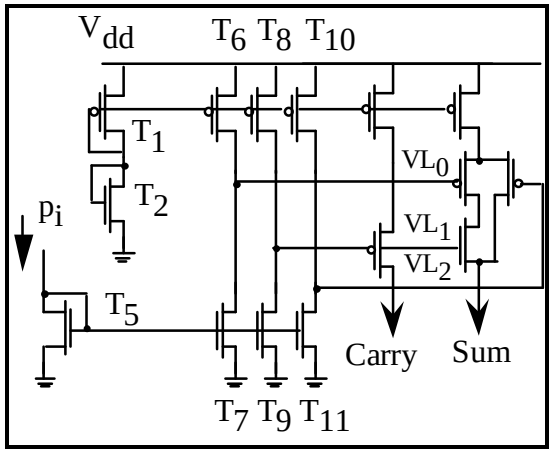


Figure 4 : 4-BC cell

2.4. Semi-analog implementation of m-BC cells.

Different schemes for 3-BC and 4-BC cells can be used if semi-analog computation is allowed. In this case, the circuits are not totally level restoring, and noise margins can be a potential issue.

Formulas for 3-BC cell are now :

$c_{i+1} = G_1(p_i)$

$w_i = p_i$ when $p_i \leq 1$ and $w_i = 0$ otherwise. We use the notation $w_i = p_i \Lambda L_1(p_i)$

Formulas for 4-BC cells are now:

$c_{i+1} = G_1(p_i)$

$w_i = p_i \Lambda L_1(p_i) + G_2(p_i)$, where + is the analog sum. This version uses 2 threshold detectors. Another option would only uses one threshold detector, where

$w_i = p_i \Lambda L_1(p_i) + \max.(0, p_i\text{-}2)$.

Figures 5 and 6 give the corresponding semi-analog 3-BC and 4-BC cells.

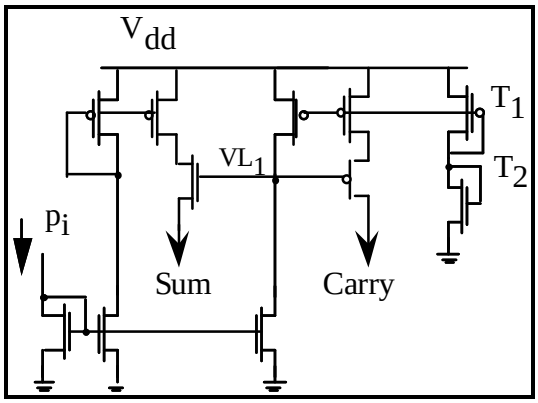


Figure 5: semi-analog 3-BC cell

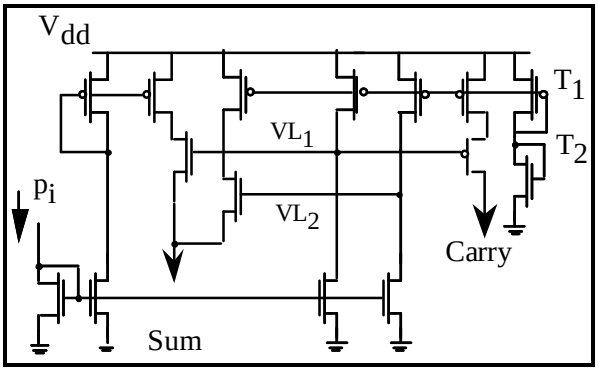


Figure 6: Semi-analog 4-BC cell

3. Circuit issues

In this section, we will consider the actual implementation of current sources and threshold detectors. In the rest of this paper, we will use the electrical parameters of the HF3CMOS technology, which is a 1.2 µm BiCMOS technology from SGS-Thomson. The basic features of the technology are given in Table 3. We only use the MOS transistors.

CMOS	NPN
NMOS (50/50) Vth : 0.7V PMOS (50/50) Vth : 1.0V BVDSS > 7V td (fin=fout) : 220 ps	Se : 3.6 x 3.6 µm2 hfe : 90 BVCEO : 14V BVCBO : 25 V BVEBO : 5V VEA : 50 V Ceb : 37.5 fF Ccb : 27 fF Ccs : 106 fF rbb' : 370 Ω ft max : 8 GHz

Table 3: HF3CMOS Technology

3.1. Implementation of current sources

In [5], depleted pMOS transistors are used to implement the current sources. With depleted MOS transistors, true current sources, that only depends on the threshold voltages can be obtained as $I_p = 1/2\mu_p C_{ox} W_p/L_p V_{tp}^2$, when connecting the transistor gate and source. But depleted pMOS transistors are not available with a standard CMOS technology.

The typical current source has been shown in figure 1. It is presented again in figure 7, with the different transistor sizes. Another one can be defined: it simply uses a p-MOS transistor, assuming that it is working in

saturated mode when a low level voltage input is applied on its gate (Figure 8).

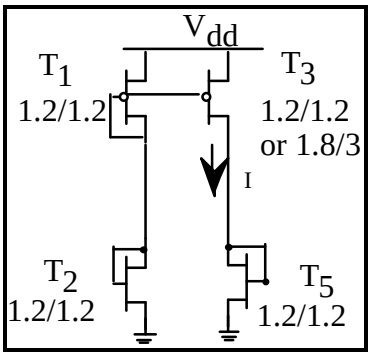


Figure 7 : current source

In figure 7, when all transistors have the minimum size (W=L=1.2µm) delivers current source 30 µA in a diode-connected minimum size transistor. When T3 has W=1.8µm and L=3µm, it delivers 20 µA. With the simplified current source (figure 8), the transistor with L=1.8 µm and W=1.2 µm delivers 60 µA in a diode-connected transistor with L=1.2 µm and W=1.8 µm.

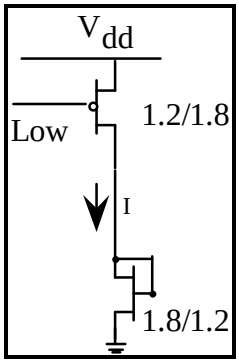


Figure 8 : simplified current source

3.2. Implementation of threshold detectors

We have first implemented the threshold detectors according to the scheme presented in figure 2. This version 0 has 0, 20 µA, 40 µA and 60 µA current levels (T3 in the current source has W=1.8 µm and L=3µm). Table 4 gives the sizes of p and n transistors for the threshold functions. It should be noticed that the transistor sizing is different than in the preliminary version presented in [1-2], where all nMOS transistors had the same size and pMOS transistors had different sizes.

We have experimented another scheme for the threshold detectors, which is presented in figure 9. The threshold function is simply implemented by a CMOS inverter, which the n transistor forms a current mirror with the transistor that sinks the input current. The voltage output of the "inverter" controls the current source, which is one of the current source defined in the previous section.

	Threshold 0-1	Threshold 1-2	Threshold 2-3
W_n/L_n	2.4/1.2	1.2/1.2	1.2/1.8
W_p/L_p	1.2/1.2	1.2/1.2	2.4/2.4
Threshold current	10µA	30 µA	50 µA

Table 4: Transistor sizes for the threshold detectors (version 0)

The version 1 with complete current sources (figure 7) has 0, 30 µA, 60 µA and 90 µA current levels. The diode connected transistor has W = 1.2 µm. Table 5 gives the sizes of p and n transistors for the threshold functions. The version 2 with simplified current sources (figure 8) has 0, 60 µA, 120 µA and 180 µA current levels. The diode connected transistor has W = 1.8 µm. Table 6 gives the sizes of p and n transistors for the threshold functions. In both cases, the threshold value is obtained by drawing the curve $I_{out} = f(I_{in})$. Figures 10 and 11 show the current transfer characteristics for version 1 and version 2. With simplified current sources, the transfer curves is not so good, because the transistor no longer operates in the saturated mode when current increases. The current value is more sensitive to current input variations.

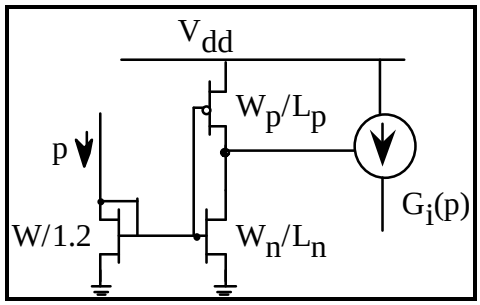


Figure 9: Threshold detector circuit.

	Threshold 0-1	Threshold 1-2	Threshold 2-3
W_n/L_n	1.8/1.8	1.8/1.2	1.2/1.2
W_p/L_p	1.2/2.4	3.6/1.2	5.4/1.2
Threshold current	18 µA	47 µA	72 µA

Table 5: Transistor sizes for the threshold detectors (version 1)

	Threshold 0-1	Threshold 1-2	Threshold 2-3
W_n/L_n	1.2/1.2	1.8/1.2	1.2/1.2
W_p/L_p	1.2/1.8	1.2/1.8	7.2/1.2
Threshold current	44 µA	84 µA	134 µA

Table 6: Transistor sizes for the threshold detectors (version 2)

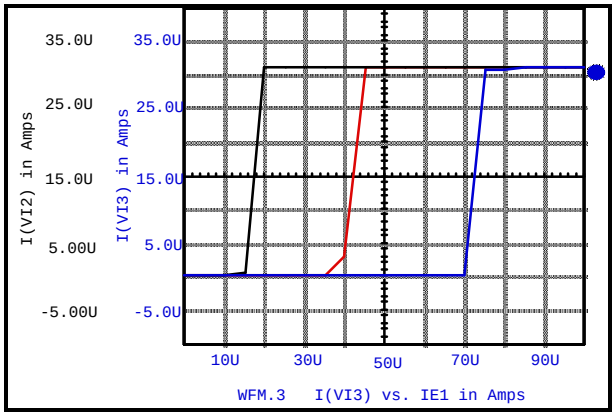


Figure 10: Threshold detector transfer characteristics (version 1)

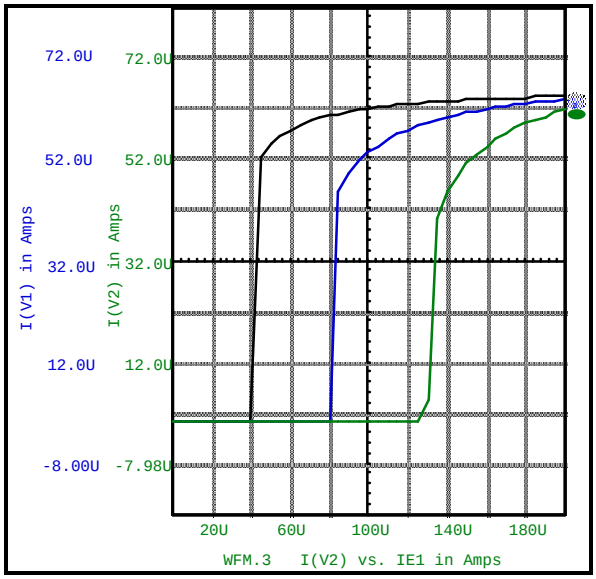


Figure 11: Threshold detector transfer characteristics (version 2).

3.3. Switching speed of threshold detectors.

Before examining the performance of the current mode adders, it is interesting to characterize the switching performance of the threshold detectors. As the outputs of the current mode full adder are given by $c_{i+1} = G_1(p_i)$ and $w_i = G_0(p_i).L_1(p_i)$, it is quite evident that the delay times for the carry and sum outputs cannot be smaller than the delay time for each of the function $G_i(p)$.

We examine three typical circuit configurations, that are shown in figure 12. For G_0, the input and output current swings are between 0 and I. For G_1, swings are between I and 2I. For G_2, swings are between 2I and 3I. It should be noticed that G_2 test circuit corresponds to the maximum output load, when 3 current sources are summed to deliver the output current. G_1 (res. G_0) test circuit gives more optimistic results as the output load is only two (res. one) current source. These test circuits give absolute minimum delay that can be expected with the actual current mode circuits.

Table 7 gives the propagation delays of G_i circuits for version 0 (original threshold detectors and true current sources). Table 8 gives the propagation delays of G_i circuits for version 1 (modified threshold detectors and true current sources) and table 9 gives the corresponding delays with version 2 (modified threshold detectors and simplified current sources). In each table, propagation delays are given for the rising edges and the falling edges.

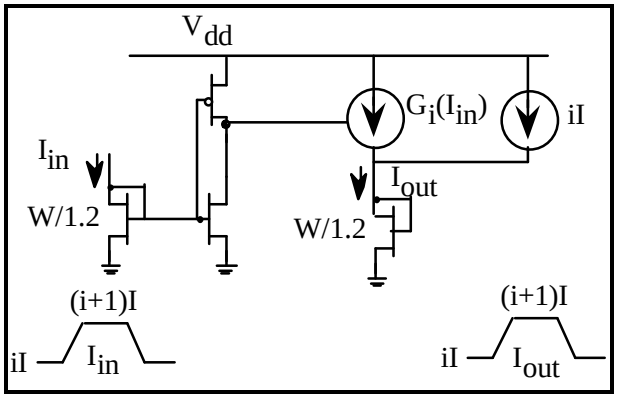


Figure 12: Test circuits for G_i propagation delay (i=0, 1, 2)

Test circuit	t_{dr} (rising edges)	t_{df} (falling edges)
G_0	3.8ns	1.8 ns
G_1	3 ns	4.2 ns
G_2	3.6 ns	6.6 ns

Table 7: G_i test circuit delays for version 0.

Test circuit	t_{dr} (rising edges)	t_{df} (falling edges)
G_0	2.6 ns	2.4 ns
G_1	1.6 ns	1.6 ns
G_2	1.6 ns	3.3 ns

Table 8: G_i test circuit delays for version 1.

Test circuit	t_{dr} (rising edges)	t_{df} (falling edges)
G_0	4 ns	1.2 ns
G_1	2 ns	2.4 ns
G_2	1.5 ns	2.4 ns

Table 9: G_i test circuit delays for version 2.

Propagation delays will be greater than 6.6 ns with version 0, 3.3 ns with version 1 and 4 ns with version 2. Although the current swing is only 50% greater with version 1 (30 µA) compared to version 0 (20 µA), version 1 is two times faster than version 0. The CMOS inverter-like threshold detector seems more efficient, as the reduced swing on the gate of the nMOS transistor is also applied on the gate of the pMOS transistor, instead of a constant voltage in the classical scheme. It can be compared with the switching speed advantage of a CMOS binary inverter versus the switching speed of nMOS inverter with depleted load.

For modified or classical threshold detectors, the propagation delays strongly depends on the W/L ratios of the transistor pairs that realize the threshold functions. The threshold values lead to W/L ratios, that give the corresponding switching speed. When the current swing is chosen and the transistor sizes are determined to implement the threshold detectors, the switching speed is determined and there is no way to improve it!

4. Performance of current mode adders

In this section, we only present performance of current mode adders which use the CMOS inverter-like threshold detectors.

4.1. Version a : true current sources - digital implementation

The first 1-bit current mode adder that has been simulated use the digital approach and the classical current source. It is presented in Figure 13. It uses 13+2 transistors. The threshold detectors have the features which have been presented in Table 5. The switching characteristics are presented in Table 10. Delay values between * correspond to switching hazards.

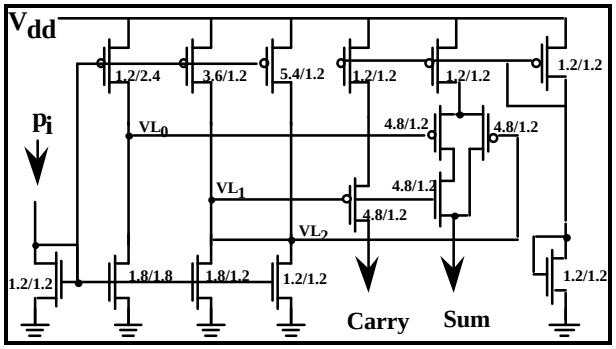


Figure 13: 1-bit current mode full adder (a)

Input	t_{sum}	t_{carry}
0-1	7 ns	----
1-2	2.4 ns 6 ns (overshoot)	2 ns
2-3	2.6 ns	-----
0-2	* 4 ns *	4 ns
1-3	* 3.6 ns *	3 ns
0-3	* 5.6 ns*	1.8 ns

Table 10 : 1-bit current mode adder (a)

4.2. Version b: simplified current sources - digital implementation

The second 1-bit current mode adder that has been simulated use the digital approach and the simplified current source. It is presented in Figure 14. It has 11 transistors. The threshold detectors have the features which have been presented in Table 6. The switching characteristics are presented in Table 11.

4.3. Version c : simplified current sources - semi-analog implementation

The third 1-bit current mode adder use the semi-analog approach and the simplified current source. It is presented in Figure 15. Only two threshold detectors are used, with following W/L ratios: 7.2/1.2 (T_p) and 1.2/1.2 (T_n) for the threshold between 120 µA and 180 µA; 2.4/1.2 (T_p) and 1.2/1.2 (T_n) for the threshold between 60 µA and 120 µA. All the other transistor sizes

can be found in Figure 15. This adder uses 11 transistors. The switching characteristics are presented in Table 12.

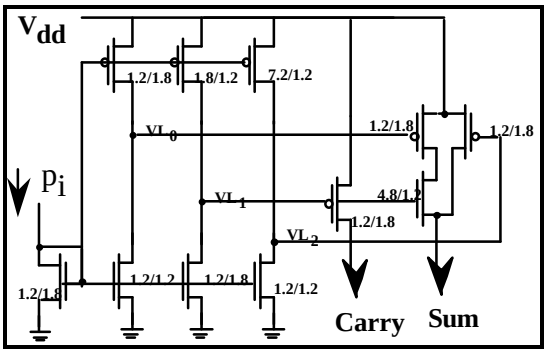


Figure 14: 1-bit current mode adder (b)

Input	t_{sum}	t_{carry}
0-1	5.8 ns	----------
1-2	4 ns	3 ns
2-3	2 ns	----------
0-2	*3.2 ns*	4.2 ns
1-3	* 5.2 ns*	3 ns
0-3	*3.6 ns*	3 ns

Table 11: 1-bit current mode adder (b)

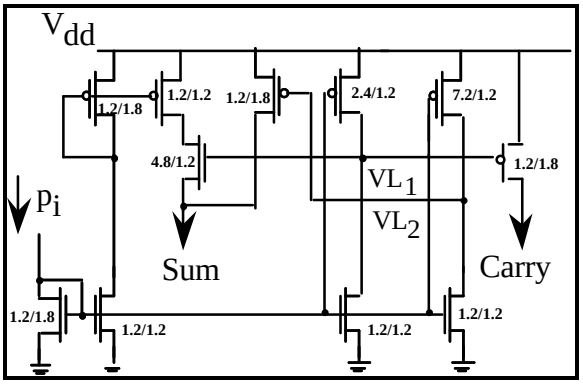
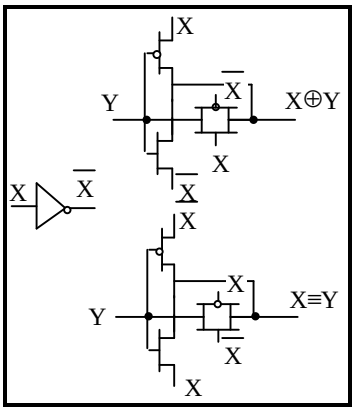


Figure 15: 1-bit current mode full adder (c)

Input	t_{sum}	t_{carry}
0-1	3.8 ns	-----
1-2	3.4 ns	2.4 ns
2-3	2 ns	-----
0-2	* 3 ns*	3.2 ns
1-3	*4.4 ns*	3 ns
0-3	* 3.5 ns*	2.2 ns

Table 12: 1-bit current mode adder (c)



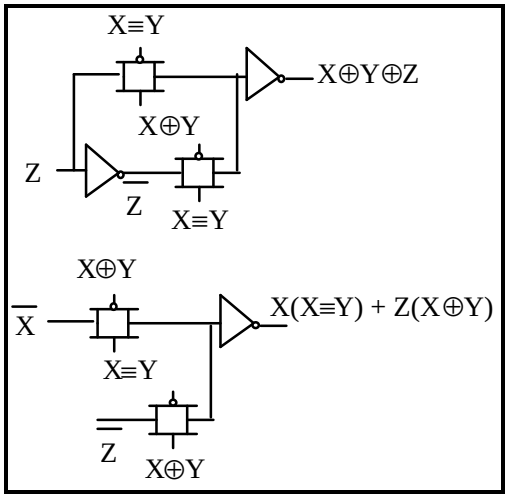


Figure 16 : Binary voltage mode CSA functional diagram.

5. Performance of the voltage mode Carry Save Adder

5.1. Circuit scheme

The voltage mode CSA, which is used for the implementation of the adder tree in combinational multiplier, is the circuit that we have used as a base for the comparison. The CSA design optimizes both sum and carry delays. The CSA scheme is given in Figure 16.

The usual semi-analog scheme, with pass transistors is used to generate the xor and the nxor functions of two inputs X and Y. A second stage generates the sum and carry outputs. Sum output is generated as $X \oplus Y \oplus Z = \overline{Z}(X \oplus Y) + Z(\overline{X \oplus Y})$ and the carry output corresponds to X when X=Y and Z when X≠Y. The CSA uses 24 transistors.

5.2. Simulation results

The CSA has been simulated with HCMOS3 parameters. All transistors have L=1.2 µm. The inverters

and pseudo-inverters use transistors with W_p = 7.2 µm and W_n = 3.6 µm. The pass transistors uses W_p = 2.4 µm and W_n = 1.2 µm. Carry and sum outputs are loaded with one xor gate. Simulation results with typical parameters and typical power supply are given in Table 13. Input configurations are indicated as "TIJ", where T means a transition, and I and J the values on the other inputs. TT (res. TTT) means a same transition on two (res. three) inputs.

Input transitions	t_{dsum}	t_{dcarry}
T00	2 ns	---
T01	2 ns	2 ns
T11	1.8 ns	--
TT0	----	2 ns
TT1	----	2 ns
TTT	1.8 ns	2 ns

Table 13 : binary voltage mode CSA performance

6. Conclusion

We have presented three different versions of current mode 1-bit adder, which propagation delays are respectively 7 ns, 5.8 ns and 4 ns with a 1.2 µm CMOS technology. These adders use 11 or 13 transistors. The propagation delays principally result on dynamic hazards (0-2, 1-3 or 0-3 transitions). They strongly depend on the input transition which occurs. Sometimes current overshoots must be considered. The corresponding binary voltage mode carry save adder uses 24 transistors (more than twice the current-mode version), but the propagation delay is limited to 2 ns, more than 2 or 3 times faster than the corresponding m-valued current mode versions. The propagation delays are nearly the same for any input transition, and there is no visible hazard, whatever the input configuration is.

With current mode circuits, the transistor sizes are fixed by the threshold values. When the sizes are fixed up, the switching speed is determined by these sizes, and there is no way to improve it. With the voltage mode circuit, the transistor sizes can be optimized to reduce propagation delays according to the capacitive loads in each node.

This study of m-valued current mode circuits, with m=4, shows that a reduced chip area can be obtained. However, the circuits have a static power dissipation, with an average current per adder which is half the maximum current level. They are several times slower than the corresponding voltage mode binary ones.

Practical uses of m-valued current mode circuits seem very difficult. To get a significant advantage at circuit architecture level, larger values of m are needed. 7-valued circuits were used in [4-5] with bi-directional current. But, tolerance issues must then be considered, and it is not so easy to implement a large number of threshold detectors with simple circuits (a transistor pair per threshold detector). On the other hand, with m = 4 (and may be m = 5), the intrinsic speed disadvantage of m-valued circuits make difficult to compete with binary circuits.

The only significant advantage of CMOS m-valued current mode circuit is chip density, when reduced operating speed is allowed. When speed is a significant factor, the attempt to use CMOS multivalued circuits looks like a dead-end.

7. References

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